IN THE CLAIMS

1. (Currently Amended) A decoding unit for decoding a turbo-code sequence, said decoding unit comprising:

a plurality of decoders for dividing a received code sequence into a plurality of blocks along a time axis, and for decoding at least two of the blocks in parallel, each decoder including a deinterleaver, an interleaver, and a decoding part.

2. (Currently Amended) The decoding unit according to claim 1, ~~wherein the received code sequence consists of a first received code sequence and a second received code sequence, wherein the first received code sequence consists of a received sequence of an information bit sequence and a received sequence of a first parity bit sequence generated from the information bit sequence, and the second received code sequence consists of a bit sequence generated by interleaving the received sequence of the information bit sequence, and a received sequence of a second parity bit sequence generated from a bit sequence generated by interleaving the information bit sequence, and wherein said decoding unit comprises~~ further comprising:

a channel value memory for storing the ~~first~~ received code sequence of the turbo-code and the received sequence of ~~the second~~ parity bit sequence of turbo-code.

3. (Currently Amended) The decoding unit according to claim 2, wherein said plurality of decoders comprise at least a first decoder and a second decoder, each of which comprises a channel value memory interface including an interleave table for reading each of the plurality of blocks of a ~~the~~ first and a second received code sequence from said channel value memory.

4. (Original) The decoding unit according to claim 3, wherein each of said plurality of decoders comprises:

a transition probability calculating circuit for calculating forward and reverse transition probabilities from channel values and prior values of each of the blocks;

a path probability calculating circuit for calculating forward path probabilities from the forward transition probabilities, and reverse path probabilities from the reverse transition probabilities;

a posterior value calculating circuit for calculating posterior values from the forward path probabilities, the reverse transition probabilities and the reverse path probabilities; and

an external value calculating circuit for calculating external values for respective information bits by subtracting from the posterior values the channel values and the prior values corresponding to the information bits.

5. (Original) The decoding unit according to claim 4, wherein each of said plurality of decoders further comprises:

means for supplying another of said decoders with one set of the forward path probabilities and the reverse path probabilities calculated finally; and

an initial value setting circuit for setting the path probabilities supplied from another decoder as initial values of the path probabilities.

6. (Currently Amended) The decoding unit according to claim 2, wherein ~~the~~ a first parity bit sequence of turbo-code and ~~the~~ a second parity bit sequence of turbo-code are punctured before transmitted, and wherein each of said decoders comprises a depuncturing circuit for inserting a value of least reliability in place of channel values corresponding to punctured bits of the received code sequences.

7. (Original) The decoding unit according to claim 4, wherein every time input of one of the blocks has been completed, each of said decoders starts decoding of the block, and output posterior values corresponding to the channel values of the block as posterior values corresponding to the information bits of the block.

8. (Original) The decoding unit according to claim 7, wherein at least one of said plurality of decoders decodes one of the blocks whose input has not yet been completed to generate posterior values of the block, and uses values corresponding to the posterior values as prior values of the block whose input has been completed.

9. (Withdrawn) A decoding unit for decoding a turbo-code sequence, said decoding unit comprising:

a decoder for dividing a received code sequence into a plurality of blocks along a time axis, and for decoding each of the blocks in sequence.

10. (Withdrawn) The decoding unit according to claim 9, further comprising a channel value memory for storing the received code sequence, wherein said decoder comprises:

a channel value memory interface for reading the received code sequence from said channel value memory block by block;

a transition probability calculating circuit for calculating forward and reverse transition probabilities from channel values and prior values of each of the blocks;

a path probability calculating circuit for calculating forward path probabilities from the forward transition probabilities, and reverse path probabilities from the reverse transition probabilities;

a posterior value calculating circuit for calculating posterior values from the forward path probabilities, the reverse transition probabilities and the reverse path probabilities; and

an external value calculating circuit for calculating external values for respective information bits by subtracting from the posterior values the channel values and the prior values corresponding to the information bits.

11. (Withdrawn) The decoding unit according to claim 10, wherein any adjacent blocks overlap each other by a predetermined length.

12. (Currently Amended) An encoding/decoding unit including an encoding unit for generating a turbo-code sequence from an information bit sequence, and a decoding unit for decoding a turbo-code sequence,

said encoding unit comprising:

a first component encoder for generating a first parity bit sequence from the information bit sequence;

an interleaver for interleaving the information bit sequence;

a second component encoder for generating a second parity bit sequence from an interleaved information bit sequence output from said interleaver; and

an output circuit for outputting the information bit sequence and the outputs of said first and second component encoders, and

said decoding unit comprising:

a plurality of decoders ~~for dividing~~ each including a deinterleaver, an interleaver, and a decoding part, the plurality of decoders configured to divide a first received code sequence and a second received code sequence into a plurality of blocks along a time axis, and for decoding at least two of the blocks in parallel, wherein the first received code sequence consists of a received sequence of ~~the~~ an information bit sequence and a received sequence of ~~the~~ a first parity bit sequence, and the second received code sequence consists of a bit sequence generated by interleaving the received sequence of the information bit sequence, and a received sequence of the second parity bit sequence; and

the decoding unit further comprises a channel value memory for storing the first received code sequence and the received sequence of the second parity bit sequence.